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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402-0938

EXAMINER	
GRAHAM, ANDREW R	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/427,815	ROSSUM, DAVID P.	
	Examiner	Art Unit	
	Andrew Graham	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *23 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/23/2005 have been fully considered but they are not persuasive. In general, it is respectfully submitted that the applicant's currently presented claim language remains broad enough in scope as to not clearly and distinctly delimit subject matter inventive in nature.

On page 9, lines 10-14, the applicant has stated, "An example of a key difference between the invention as claimed in claim 1 and the teachings of Chester and related prior art is that the present invention allows, within a single architecture, the selection of an arbitrary sample rate ratio, and the capability to arbitrarily vary that ratio on an output sample by output sample basis. Thus, the sample rate may be controllably varied". The examiner respectfully submits, however, that any such difference is not clearly conveyed by the presently submitted claim language. Chester teaches that the sampling rate change includes fractions with numerator and denominator of intermediate size (col. 3, lines 1-5). The implementation of such a fraction or the factors (L/M) of expansion or decimation corresponding thereto meet the concept of a "selection" as presented in the above cited remarks as far as such a "selection" pertains to the submitted claim language. The implementation of such a desired one sampling rate, however, is capable of varying to other, different output sample rates as an effect of jitter, as is evidenced by the document of Pohlmann. The claim language of each of the independent

claims only requires that such varying be capable, as opposed to actually being formally or otherwise implemented. As evidenced by the document of Pohlmann, the signal being processed by Chester is digital and thus it is inherent that the phenomenons of drift or jitter possibly occur. Accordingly, the teachings of Chester, in view of the inherent properties of such a system, are considered to teach the "capability" in the above cited remarks, so far as such a capability is represented in the corresponding claim language. Regarding the amended qualifier of "controllably varied", Pohlmann also discloses that a phase locked loop (PLL) may be used to control jitter based on a feedback comparison of the phase of an input signal with itself. Again, as the processed signal of the system of Chester is a digital signal, it is possible to incorporate a jitter control device, such as the shown PLL in Pohlmann, and the involved function as part of the processing of the output signal.

On page 10, lines 1-2, the applicant has stated, "Clearly, Chester's disclosed architectures are each described as converting a signal to one and only one output sample rate". The examiner respectfully submits, however, that such an interpretation of Chester does not overcome or render distinct the pertinent claim language, even with a limited consideration of the inherent properties of Chester's system. Considering, for example, Claim 1 the pertinent claim language is "varying said input sample rate associated with said input signal to any one of the plurality of differing output sample rates". The central effect or requirement of this claim limitation is

the step rephrased as "varying the input sample rate to any *one* output sample rate". The effect of the prepositional phrase "of the plurality of differing output sample rates", while providing context or a characteristic of the "any one" rate, does not require that the input same rate ever be varied to a different or alternate rate than, for example, the exact rate of L or M or L/M designated in the teachings of Chester. The clause of "of said plurality of differing output sample rates", as applied in the final lines of the claims, delimits the property that the output sample rate must be "capable of being controllably varied to any one of said plurality of differing output sample rates for any output data sample". As such, this capability is a property of that, while possible, does not need to be expressly implemented as part of operation of the system. The source or basis of these "plurality of different output sample rates" is not further specified in the claims, allowing a broadest, reasonable interpretation of said plurality of differing output sample rates to include those that would be affected as jitter. As the output signal of Chester is a digital signal, the reference of Pohlmann supports the notion that an implemented output sample rate may be varied at each output sample, as is generally illustrated in Figure 3-8 of Pohlmann. Regarding the amended phrase "controllably varied", the teachings of Pohlmann illustrate that jitter control is known in the art. Pohlmann teaches an example of a PLL circuit that can decrease the jitter or sample rate variations to accepted tolerances. Accordingly, as the output signal of Chester is a digital signal, the reference of

Pohlmann supports the notion that an implemented output sample rate may be controllably varied at each output sample though the use of a PLL circuit in the resampling circuit that creates a 'pure enough' sampling clock for use by the resampling circuit. Thus, it is respectfully submitted that the amended limitations yet remain an inherent property of the digital processing circuit of Chester, as evidenced by Pohlmann.

On page 10, lines 9-11, the applicant has stated, "He then reiterates in lines 50-51 that the output frequencv Fout equals LxFin. This makes it crystal clear that Chester in no way anticipates varying the input sample rate at all". Reviewing the same citations, it is respectfully submitted that the applicant's derivation of the conclusion in the above citation (that the input sample rate is unvaried, to paraphrase) is unclear. Lx is an interpolation rate, implemented by sample rate converters (col. 2, lines 66-67). An example of such a sample rate expansion is given as "31" (col. 7, lines 15-27). When, given the equation (Fout equals Lx*Fin) in the above citation by the applicant, applying an Lx of "31" results in Fin*31=Fout, which illustrates that Fin does not equal Fout, or alternately stated, the sampling rate of the input signal has been changed in comparison with the sampling rate of the signal upon input into the system. The applicant further states on page 10, lines 12-14 that "Chester and all the related prior art is aimed at devices that change an input signal at one input sample rate to another signal at an output sample rate that is a fixed ratio to the input sample rate".

It is respectfully submitted that this statement contradicts the above cited statement, as such a change, even if it is a fixed ratio, is a form of "varying".

On page 11, lines 1-5, the applicant has stated, "If jitter is to be invoked as the mechanism by which the output sample rates are to be varied, it must be that the jitter varies the output rate among said plurality of output rates that were referenced in the initial limitation of the claim". The examiner respectfully submits that, as evidenced by the citation of "*said* plurality of differing output sample rates" in the previous and current office actions, this was the interpretation afforded to the pertinent claim limitations in the current and previous rejections. As a whole, Chester specifically teaches "varying" to one of a plurality of differing output sample rates, wherein the plurality of sample rates are an output capability as an inherent property of the system.

On page 11, lines 7-10, the applicant has stated, "Applicant submits that the only reference to slowly varying sample rates is in the detailed description of the present application where it is disclosed that the input to output sample rate ratio L/M can vary slowly with time". The examiner respectfully disagrees. Line 8 of page 2 of the applicant's specification states "L and M are integers which can slowly change with time". L and M are the values that determine the new sampling rate. This reference to the "slow change with time" property of these integers is made in the context of a "classical" multi-stage converter algorithm. Accordingly, such a time

varying property is part of the applicant's admitted prior art, and not disclosed solely in the applicant's detailed description. Additionally, Pohlmann teaches drift or "slowly-varying deviations" (page 123).

Claim Rejections - 35 USC § 112

2. The applicant's amendments made to Claims 17-22 in view of the previous rejection(s) under 35 U.S.C. 112 of said claims suffice to overcome the basis of said rejection(s). Accordingly, said rejections are hereby withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-10 and 12-31** are rejected under 35 U.S.C 102(b) as being anticipated by Chester (USPN 5717617).

Chester discloses a system for using multiple stages of signal processing to increase or decrease the sampling rate of an input signal. The architecture is applicable to both decimation and interpolation, which reads on "A method for converting an input signal to one of a plurality of differing output sample rates" (col. 2, lines

23-27). Figure 7b illustrates a first interpolating or upsampling embodiment of the disclosed invention. The illustrated system operates on a digital input signal with an associated input frequency f_{IN} (col. 6, lines 50-52). This input sampling frequency of the input signal reads on "receiving, at an input sample rate, a plurality of data points, associated with the input signal". The first stage of the signal processing includes a low pass filter (LPF1), which has an associated transition band shown in Figure 8b (col. 6, lines 60-64). Figure 8c illustrates the images resulting from this filtering. The second stage of the shown processing also involves a low pass filter (LPF2) and Figure 8d (col. 7, lines 6-10). The application of either of these two filters and the shown two stages to the input signal reads on "operating on said plurality of data points to associate said input signal with a predetermined set of parameters, with said set of parameters including a first transition band having an image corresponding thereto". The third stage of the processing involves an interpolation by a factor (L_2) and a third filtering (LPF3) (col. 6, lines 56-67). In view of the inherent properties of a digital system, as further discussed below, the upsampling performed by the interpolation (L_2) reads on "varying said input sample rate associated with said input signal to any one of a plurality of differing output sample rates by interpolation with an interpolator". The width of the transition band of the third filter is shown in Figure 8e (col. 7, lines 10-14). The width of this transition band can be seen comparatively in Figures 8b and 8c, which show that the transition

band of the third filter (LPF3) is twice that of the first filter (LPF1), and it happens to extend up to the base of the first, non-filtered harmonic image, which is related to the stop band of the second filter. Thus, the third filter reads on "having associated therewith a second transition band, with the width associated with said second transition band being a function of a spectral separation of said first transition band and said image". The final processed signal has an adjusted frequency of F_{OUT}, which reads on "an output signal is produced having a sequence of data samples approximating the input signal" (col. 6, lines 50-55).

Chester teaches that system is implemented in the context of semiconductor circuits as well as A/D and D/A conversion (col. 1, lines 17-27). Jitter is a phenomenon capable of occurring during the processing of a signal, including functions such as the sampling of a signal. Jitter can occur as random variations in a clock edge or periodically. Drift is a slow-varying deviation that may occur in the interconnection of components. The reference of Pohlmann, pages 57-60 and 122-127, has been provided with this office action to ascertain that jitter and drift are well known phenomenon in the art. Pohlmann also teaches that jitter may be adjusted to a "pure enough" or within tolerance degree through the use of a phased locked loop (PLL)(page 123). Such a feedback, comparison based system (the PLL) provides evidence to the fact that jitter in a sampling system may be "controllably varied". As the system of Chester is a digital signal processing system that is disclosed in the context of A/D conversion

and sequential digital processing of a signal by components, the throughput of the disclosed systems of Chester is inherently "capable of being controllably varied to any one of said plurality of differing output sample rates for any output data sample" by virtue of the possible presence of drift. It is further noted that the applicant has disclosed the concept of a slowly varying sample rate in the context of admitted prior art (page 2, lines 6-8 of originally filed specification).

Regarding **Claim 2**, Chester discloses that the low pass filters are of FIR type, with 128, 140, and 128 taps, which has collectively fewer taps than traditional one stage FIR filtering (col. 5, lines 63-67 and col. 6, lines 1-9). FIR structures are well known in the art to apply coefficients to sequential values of the input sample values, as is noted by Chester (col. 4, lines 1-34). The use of these filters reads on "convolving a predetermined finite number of N data points with an equal number of coefficients, with N being greater than two".

Regarding **Claim 3**, Chester notes that the coefficients of an FIR filter, as is well known in the art, are time varying (col. 4, lines 29-31). This reads on "coefficients vary as a function of the temporal spacing between the output point and the corresponding input points".

Regarding **Claim 4**, Chester discloses an interpolation embodiment with a particular expansion rate (col. 6, lines 33-45). The overall rate change of this embodiment reads on "varying said input sample rate increases said input sample rate".

Regarding **Claim 5**, Chester discloses a decimation embodiment of the sample rate conversion system (col. 4, lines 38-40). This reads on "varying said input sample rate decreases said input sample rate".

Regarding **Claim 6**, the interpolation rate of the interpolator of the first stage of the processing shown in Figure 7b includes selectable factors (col. 6, lines 46-50). Chester discloses that the two interpolators in the shown embodiment have a combined target interpolation factor, and that the first interpolation factor is the smaller of the two (col. 6, lines 46-50). The example given includes this factor as three, with the overall interpolation factor being 31 (col. 7, lines 15-24). These teachings, in view of a smaller potential interpolation factor, read on "upsampling said data points by a factor of two".

Regarding **Claim 7**, the width of the transition band of the first low pass filter is half of the frequency of interpolation rate (L_2) (col. 60-64). This reads on "filtering said plurality of data points with a half band filter".

Regarding **Claim 8**, the interpolation embodiment involves the use of a decimator (L_2) with the first stage low pass filter (col. 6, lines 60-67). This reads on "operating on said plurality of data points includes decimating said plurality of data points with a half-band decimator".

Regarding **Claim 9**, Chester discloses an embodiment of a rate change system in Figure 9. This embodiment can be seen to comprise a series of stages of interpolating and filtering. The third stage is

disclosed as having a transition band that extends to .0838 F_1,which is the same frequency of the end of the transition band of the first low pass filter (LPF1) (col. 8, lines 19-22 and 39-40). The transition band of the filter of the first stage extends to half of an intermediate frequency (Figure 10A). The third stage, which includes decimation, thus reads on "decimating a plurality of data points output by said interpolator with a half band decimator". This stage occurs after the input of the signal to be processed, and after the interpolation performed in the first stage, which reads on "varying said input sample rate occurring after receiving said plurality of data points and before decimating said plurality of data points" (Figure 9).

Regarding **Claim 10**, please refer to the above discussion of the parallel limitations of Claim 2, noting Chester's discussion of prior art FIR filters and the number of taps in the involved filters (col. 1, lines 40-54; col. 4, lines 27-34; col. 6, lines 1-9).

Regarding **Claim 12**, please refer to the above discussion of the parallel limitations of Claims 1 and 7, noting that Chester discloses the selection of the interpolation rate (col. 6, lines 46-50).

Regarding **Claim 13**, please refer to the above discussion regarding the parallel limitations of Claims 6 and 7, and the first stage of the processing of Chester in Figure 7b.

Regarding **Claim 14**, Chester discloses an embodiment of a rate change system in Figure 9. This embodiment can be seen to comprise a series of stages of interpolating and filtering. The second and

fourth filters (LPF2, LPF4) can be seen to not involve any interpolation or decimation, and their transition bands extend to half of the relative sampling frequencies (col. 8, lines 24-26 and 50-54). This reads on "said halfband filtering is done, without upsampling, on said plurality of data points". The third and fifth stages of the system can both be seen to include interpolation, which reads on "said interpolating follows said halfband filtering".

Regarding **Claim 15**, in view of the interpolation performed in the third stage of Figure 9 of Chester, the filtering discussed in the fourth stage as discussed above in regards to Claim 16, reads on "additional halfband filtering follows said interpolating" (col. 8, lines 50-54).

Regarding **Claim 16**, the transition band in the first stage of Figure 9, which includes an upsampling part with a factor of (L_X) can be seen in Figure 10A to be half an intermediate frequency, which reads on "said halfband filtering is performed in conjunction with upsampling said plurality of data points" (col. 8, lines 13-23). The interpolation performed in the third stage reads on "said interpolating follows said halfband filtering" (Figure 9). The halfband filtering of the fourth stage, which is discussed above in regards to Claim 14, and the decimation performed in the fifth stage read on "halfband filtering and decimating follow said interpolating".

Regarding **Claim 17**, please refer to the above discussion of similar limitations in Claim 1, noting that microprocessors, which operate on code, are one, well-known format of a semiconductor circuit

that performs digital signal processing.

Regarding **Claim 18**, please refer to the above discussion of similar limitations in Claim 6.

Regarding **Claim 19**, please refer to the above discussion of similar limitations in Claim 7.

Regarding **Claim 20**, please refer to the above discussion of similar limitations in Claim 8.

Regarding **Claim 21**, please refer to the above discussion of similar limitations in Claim 9.

Regarding **Claim 22**, please refer to the above discussion of similar limitations in Claim 10.

Regarding **Claim 23**, please refer to the above discussion of similar limitations in Claim 12, noting the storage disclosed by Chester and inherent for the digital implementation of the system (col. 9, lines 61-64).

Regarding **Claim 24**, please refer to the above discussion of similar limitations in Claim 13.

Regarding **Claim 25**, please refer to the above discussion of similar limitations in Claim 14.

Regarding **Claim 26**, please refer to the above discussion of similar limitations in Claim 15.

Regarding **Claim 27**, please refer to the above discussion of similar limitations in Claim 16.

Regarding **Claim 28**, Chester teaches the use of a weighted sum of sequential samples wherein the weighting coefficients are periodically

time varying (col. 4, lines 14-22 and Figure 4c). This reads on "wherein said interpolator is an FIR Nth order sum of products interpolator with linear interpolation of coefficients".

Regarding **Claim 29**, please refer to the above discussion of similar limitations in Claim 28.

Regarding **Claim 30**, Figure 8e illustrates that the transition band of the third filter extends to the base of a harmonic image, which reads on "said interpolator has a transition band beginning adjacent the top of a passband and ending adjacent the bottom of a passband image" (col. 7, lines 10-14).

Regarding **Claim 31**, please refer to the above discussion of similar limitations in Claim 30.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 11, 22, 31, and 32** are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chester applied above, and in further view of White (USPN 5808924).

As detailed above, Chester discloses a system for using multiple

stages of interpolation, filtering, and decimation for various sample rate conversions of an input signal.

However, Chester does not specify:

- that the involved filters are infinite impulse response filters

White discloses a decimating IIR filter. This filter involves an integrate and dump circuit (50) and a output loop (52) (col. 4, lines 33-36). The integrate and dump circuit involves a single feedback loop connected through an adder that involves a delay element (col. 4, lines 39-48). The output loop involves a multiplying element and a delay element (col. 4, lines 49-59). This overall combined system, shown in Figure 4, reads on "filtering the same with an infinite impulse response filter".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious it would have been obvious to utilize the IIR decimating filter in the processing stages discussed above in the system of Chester. The motivation behind such a modification would have been that such an IIR filters would have required fewer components and circuitry than the multi-tap FIR filters of Chester. IIR filters are also well known in the art to involve more input samples in the signal adjustment process than FIR filters.

Regarding **Claim 22**, please refer to the above discussion of similar limitations in Claim 11.

Regarding **Claim 32**, the system of White utilizes first order all-pass sections, which, in view of the filtering of Chester, reads on

"said halfband filter is an IIR filter composed on first order allpass blocks" (col. 2, lines 20-22 and col. 3, lines 29-33).

Regarding **Claim 33**, please refer to the above discussion of similar limitations in Claim 32.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Graham whose telephone number is 571-272-7517. The examiner can normally be reached on Monday-Friday, 8:30 AM to 5:00 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7848.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Graham
Examiner
A.U. 2644
Ag
ag

July 29, 2005

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600